Listing of Claims:

1. (Currently Amended) A wafer-interposer assembly comprising:

a semiconductor wafer including a plurality of semiconductor die, each semiconductor die having a plurality of first electrical contact pads;

an interposer ~~non-temporarily~~ electrically connected and mechanically ~~connected~~ secured to the semiconductor wafer, the interposer including a plurality of second electrical contact pads respectively electrically connected and mechanically secured to at least some of the first electrical contact pads via ~~conductive attachment elements~~ soldered connections such that the interposer and the semiconductor wafer are operable to be singulated into a plurality of chip assemblies, each chip assembly comprising a semiconductor die and a portion of the interposer electrically connected and mechanically secured to one another via soldered connections; and

a communication interface integrally associated with the interposer and electrically connected to at least some of the second electrical contact pads.

2. (Original) The wafer-interposer assembly as recited in claim 1 wherein the communication interface further comprises an integral edge connector with pins.

3. (Original) The wafer-interposer assembly as recited in claim 1 wherein the communication interface further comprises an integral bayonet connector with pins.

4. (Original) The wafer-interposer assembly as recited in claim 1 wherein the communication interface further comprises a connector added to the wafer-interposer assembly.

5. (Original) The wafer-interposer assembly as recited in claim 1 wherein the communication interface further comprises soldered connections.

6. (Original) The wafer-interposer assembly as recited in claim 1 wherein the communication interface further comprises a ribbon connector.

7. (Original) The wafer-interposer assembly as recited in claim 1 wherein the communication interface further comprises an RF connector.

8. (Original) The wafer-interposer assembly as recited in claim 1 wherein the communication interface further comprises an optical connector.

9. (Original) The wafer-interposer assembly as recited in claim 1 wherein the communication interface further comprises a transmit/receive antenna.

10. (Original) The wafer-interposer assembly as recited in claim 1 wherein the communication interface further comprises a quick release device.

11. (Original) The wafer-interposer assembly as recited in claim 1 wherein the communication interface is operably coupled to a testing apparatus that tests at least some of the semiconductor die prior to the singulation of the interposer and the semiconductor wafer.

12. (Original) The wafer-interposer assembly as recited in claim 1 wherein the communication interface is operably coupled to a testing apparatus that burn-in tests at least some of the semiconductor die prior to the singulation of the interposer and the semiconductor wafer.

13-25. (Canceled)

26. (Currently Amended) A wafer-interposer assembly comprising:

a semiconductor wafer including a plurality of semiconductor die having a pattern of first electrical contact pads disposed thereon;

an interposer electrically connected and mechanically secured to the semiconductor wafer, the interposer having a first surface with a pattern of second electrical contact pads disposed thereon, at least some of which correspond to and are ~~non-temporarily~~ electrically connected and mechanically ~~connected~~ secured to at least some of the first electrical contact pads via ~~conductive attachment elements~~ soldered connections, the interposer also having a second surface having a pattern of third electrical contact pads that are electrically connected to at least some of the second electrical contact pads, such that the interposer and the semiconductor wafer are operable to be singulated into a plurality of chip assemblies, each including a semiconductor die and a portion of the interposer that remain electrically connected and mechanically secured to one another via soldered connections; and

a communication interface integrally associated with the interposer and electrically connected to at least some of the second electrical contact pads.

27. (Previously Presented) The wafer-interposer assembly as recited in claim 26 wherein the communication interface further comprises an integral edge connector with pins.

28. (Previously Presented) The wafer-interposer assembly as recited in claim 26 wherein the communication interface further comprises an integral bayonet connector with pins.

29. (Previously Presented) The wafer-interposer assembly as recited in claim 26 wherein the communication interface further comprises a connector added to the wafer-interposer assembly.

30. (Previously Presented) The wafer-interposer assembly as recited in claim 26 wherein the communication interface further comprises soldered connections.

31. (Previously Presented) The wafer-interposer assembly as recited in claim 26 wherein the communication interface further comprises a ribbon connector.

32. (Previously Presented) The wafer-interposer assembly as recited in claim 26 wherein the communication interface further comprises an RF connector.

33. (Previously Presented) The wafer-interposer assembly as recited in claim 26 wherein the communication interface further comprises an optical connector.

34. (Previously Presented) The wafer-interposer assembly as recited in claim 26 wherein the communication interface further comprises a transmit/receive antenna.

35. (Previously Presented) The wafer-interposer assembly as recited in claim 26 wherein the communication interface further comprises a quick release device.

36. (Previously Presented) The wafer-interposer assembly as recited in claim 26 wherein the communication interface is operably coupled to a testing apparatus that tests at least some of the semiconductor die prior to the singulation of the interposer and the semiconductor wafer.

37. (Previously Presented) The wafer-interposer assembly as recited in claim 26 wherein the communication interface is operably coupled to a testing apparatus that burn-in tests at least some of the semiconductor die prior to the singulation of the interposer and the semiconductor wafer.